Form PTO-1449 Sheet 1 of 3

Applicant: Venna et al.

Serial No.: 10/691,376 Att'y Docket No.: 15436.247.51.1

Filing Date: October 22, 2003 Group: Unknown

For: OPTOELECTRONIC SEMICONDUCTOR DEVICE

OIPE JC156 NOV 24 2003 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATIONS MADE BY APPLICANT

U.S. Patent Documents

Examiner Initial*	Document Number	Issue Date	Name
DM 1	3,467,906	09/16/69	Cornely et al.
DM 2	3,828,231	08/06/74	Yamamoto
DM 3	4,794,346	12/27/88	Miller
DM 4	5,305,412	04/19/94	Paoli
DM 5	5,436,759	07/25/95	Dijaili et al.
DM 6	5,604,628	02/18/97	Parker et al.
DM 7	5,805,322	09/08/98	Tomofuji

Foreign Patent Documents

Examiner Initial*	Document Number	Publication Date	Country or Patent Office
DM 8	56006492	01/23/81	Japan
DM 9	01129483	05/22/89	Japan

Examiner: [signature] Date Considered: 7/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Documents
(including author, title, pertinent pages, etc.)

Examiner Initial*

DM 10 *"A Gain-Clamped, Crosstalk Free, Vertical Cavity Lasing Semiconductor Optical Amplifier for WDM Applications,"* by J.D. Walker, F.G. Patterson, S.P. Dijaili, R.J. Deri, Lawrence Livermore National Library

DM 11 *"Gain Optimization in Switches Based on Semiconductor Optical Amplifiers,"* by Gibong Jeong and Joseph W. Goodman, IEEE Journal of Lightwave Technology, Vol. 13, No. 4, April 1995

DM 12 *"Spot-Size Converted Polarization-Insensitive SOA Gate with a Vertical Tapered Submicrometer Stripe Structure,"* by N. Yoshimoto, K. Magari, T. Ito, Kawaguchi, K. Kishi, Y. Kondo, Y. Kadota, O. Mitomi, Y. Yoshikuni, Y. Hasumi, Y. Tohmori and O. Nakajima, IEEE Photonics Technology Letters, Vol. 10, No. 4, April 1998

DM 13 *"Spot-Size Converter Integrated Semiconductor Optical Amplifiers for Optical Gate Application,"* by Shotaro Kitamura, Hiroshi Hatakeyama, Kiichi Hamamoto, Tatsuya Sasaki, Keiro Komatsu and Masayuki Yamaguchi, IEEE Journal of Quantum Electronics, Vol. 35, No. 7, July 1999

Examiner: [signature] Date Considered: 7/05

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References Cited by Applicants

While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

Each citation initialed by the Examiner will be printed on the issued patent in the same manner as references cited by the Examiner on Form PTO-892.

The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

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